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UNITED STATES PATENT APPLICATION

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FOR

DUAL DIELECTRIC STRUCTURE FOR SUPPRESSING LATERAL
LEAKAGE CURRENT IN HIGH FILL FACTOR ARRAYS

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FIELD OF THE INVENTION

The present invention relates generally to the structure of a full fill factor image array and its method of manufacture, and more particularly to the structure of a full fill factor image array that reduces lateral leakage current and its method of manufacture.

BACKGROUND OF THE INVENTION

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A conventional image array is typically formed of a plurality of photosensitive elements or pixels arranged in rows and columns. A conventional photosensitive element is shown in FIG. 1. Each photosensitive element (10) comprises photosensitive island (12) of amorphous silicon (a-Si) over a bottom contact pad (14) over a substrate (11). A transparent upper conductive layer (16) of indium tin oxide (ITO) resides over the assembly. A passivation layer (18) is disposed under the ITO (16) except where the ITO is in electrical contact with the upper surface of the of the photosensor island (12). The photosensitive element further includes a N+ doped region (22) and a P+ doped region (24). A conventional passivation layer (18) comprises an oxyinitride layer (26) and a polyamide layer (28).

In contrast to the conventional image arrays in which each pixel is defined by a stand alone PIN photosensitive element, the full fill factor image array improves the pixel fill factor by using continuous layers of amorphous silicon (a-

Si) and P+ doped a-Si. The pixels in a high fill factor array are defined only by a mushroom shaped collection electrode.

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A conventional full fill factor image array is shown in FIG. 2. The full fill factor image array (40) includes a plurality of source-drain metal contacts (44) on a substrate (42). For ease of description, other elements that may be formed on the substrate, such as gate lines, data lines, and thin film transistors (TFTs) are not shown. The source-drain metal contacts (44) are formed of an electrically conductive material such as a molybdenum ~~or~~ chromium alloy. They typically comprise one or more layers of metal. The source-drain metal contacts (44) are electrically connected to the switching and processing circuits (not shown).

To increase the area of carrier collection, a patterned mushroom-shaped collection electrode (46) is provided over the source-drain metal (44). Disposed on top of the mushroom shaped collection electrode is an N+ doped a-Si layer (48).

In contrast to a conventional image array using stand alone PIN photosensitive elements, the full fill factor image array uses a continuous intrinsic amorphous silicon (i a-Si) layer (50) and a continuous P+ doped a-Si layer (52). An upper electrode (54) of ITO resides on top of the P+ doped a-Si layer.

A conventional passivation layer comprises an oxynitride layer (56) deposited to thickness of about 1 micron by plasma enhanced chemical vapor deposition (PECVD). The passivation layer serves as the insulation between the source-drain metal (44) and photosensor (46, 48, and 50)

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Like conventional photosensitive elements, the sensor structure of conventional full fill factor image arrays suffers from intrinsic leakage. Intrinsic leakage (58), represented in FIG. 2, arises due to material defects rather than the structure of the photosensitive element. The intrinsic leakage current of a 60 x 60 μm^2 stand alone PIN sensor, for example, is about 2 femto-amps (fA). In addition to intrinsic leakage, however, the conventional full factor image array structure suffers lateral leakage between pixels. This lateral leakage current causes image blurring effects and severely reduces the imager performance. The lateral leakage current for a 60 x 60 μm^2 full fill factor array may be as high as 0.3 pico-amps (pA) at 5 V.

The bulk conductivity of high quality intrinsic a-Si is less than $10^{-11} (\Omega \cdot \text{cm})^{-1}$ which is about $2 \times 10^{14} \Omega$ between a 60 x 60 μm^2 pixel and its neighbor. Therefore, the intrinsic bulk conductivity of a-Si cannot be responsible for the high lateral leakage current. The most likely conducting mechanism for this lateral leakage current is conduction through the accumulated charge in the a-Si and oxynitride interface. Both the trapped positive ion in the oxynitride and the interface states in the a-Si/oxynitride interface can cause electron accumulation in the a-Si/oxynitride interface, creating a conducting channel between pixels.

One solution is to replace the passivation layer with another dielectric material such as silicon oxide or silicon nitride. Deposition rates for silicon oxide or silicon nitride, however, are usually much lower than for oxynitride. Therefore, deposition of a silicon nitride or silicon oxide passivation layer of about 1 micron

would be impractical. In addition, other problems such as stress build-up may degrade the sensor structure.

In light of the foregoing, there is a need for a method and structure to reduce the lateral leakage current in full fill factor sensor arrays.

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SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a high fill factor image array including a plurality of source-drain metal contacts disposed in an image array pattern, a dual dielectric passivation layer that suppresses lateral leakage current comprising a first passivation layer and a second passivation layer
10 deposited over the first passivation layer, wherein the thickness of the second passivation layer is less than the thickness of the first passivation layer, a continuous layer of a-Si, a plurality of a patterned collection electrodes disposed on top of the source-drain metal contacts, a first doped silicon layer disposed over the collection electrodes a continuous second doped silicon layer, and an
15 upper electrode.

In another aspect, the invention is directed to a method for making a high fill factor image array including the steps of providing a plurality of source-drain metal contacts, depositing a first passivation layer, depositing a second passivation layer that suppresses lateral leakage current, opening a plurality of
20 via holes through the first and second passivation layers, depositing a layer of conductive material, depositing a first doped a-Si layer, patterning to form the

collection electrodes, depositing a continuous layer of i a-Si, depositing a continuous second layer of doped a-Si, depositing and patterning an upper conductive layer.

It is to be understood that both the foregoing general description
5 and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

The accompanying drawings are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention and together
10 with the description serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, serve to explain the objects, advantages, and principles of
15 the invention.

FIG. 1 is schematic cross sectional view of a prior art PIN photosensitive element.

FIG. 2 is schematic cross sectional view of a prior art full fill factor sensor array.

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FIG. 3 is schematic cross sectional view of a dual dielectric passivation structure in a full fill factor sensor array according to one embodiment of the present invention.

FIG. 4 is a plot of current versus voltage that shows the measured leakage current for a conventional sensor array and a sensor array with a dual dielectric passivation layer.

FIGS. 5a-d are cross-sectional views that schematically illustrates the steps in making the image array with the dual dielectric passivation layer according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

FIG. 3 illustrates the components of a full fill factor sensor array formed in accordance with the principles of the present invention. According to one aspect of the invention, the fundamental components of an a full fill factor sensor array (140) include a plurality of source-drain metal contacts (144) arranged in rows and columns, a plurality of patterned mushroom shaped metal contacts (146) over the source-drain metal contacts, N+ doped a-Si regions (148) over the mushroom shaped collection electrodes (146), and a dual passivation layer (156, 157). The full fill factor sensor array further includes continuous layers of i a-Si

(150) and P+ doped a-Si (152). An upper electrode layer (154) of, for example, ITO is disposed on top of the P+ a-Si layer.

The dual passivation layer (156, 157) includes a first dielectric layer (156) of a material that is an insulator, has a low dielectric constant to minimize capacitive coupling between the contacts, and is low stress to prevent cracking. Examples of passivation materials include silicon oxynitride, benzo-cyclo-butene (BCB), or polyimides. The thickness of the first passivation layer (156) depends on the material used and can be, for example, 1 to 5 μm . A first passivation layer (156) is preferably oxynitride with a thickness of about 1 micron.

A second dielectric layer (157) of, for example, an oxide or nitride is then deposited over the first dielectric layer. The thickness of the second dielectric layer (157) is not critical, but should be thinner than the first passivation layer. Preferably, the second passivation layer (157) should be a oxide with a thickness of about 1000 Å.

The dual dielectric passivation layers' (156, 157) effect on the lateral leakage current is demonstrated in FIG. 4. Lateral leakage current was directly measured on test arrays comprising 60 μm square pixels, 20 μm apart. In one test array a 1 micron thick oxynitride passivation layer was deposited. In a second test array, a dual dielectric passivation structure comprising a 1 micron thick oxynitride layer and a high quality oxide layer with thickness of about 1000 Å was deposited. In order to isolate the lateral leakage current out of the total leakage current which includes intrinsic leakage current and lateral leakage

current, the P+ a-Si and ITO layers were not deposited on either test array. As shown in FIG. 4, the test array with the conventional oxynitride passivation layer showed a lateral leakage current as high as 0.3 pA at 5 volts. The measured lateral leakage current for the dual dielectric passivation structure according to one embodiment of the present invention is about 4 fA at 5V. Thus, the dual passivation layer structure reduces lateral leakage current by about two orders of magnitude over the conventional structure.

The method of making the image array with the dual dielectric passivation layer according to one embodiment of the present invention is shown in FIGS.

5a-e. As shown in FIG. 5a, the first passivation layer (156) is deposited over the source drain metal contact (144) and a substrate (not shown) that includes gate lines (not shown), data lines (not shown), and switching circuits such as, for example, thin film transistors (TFT). The thickness of the first passivation layer (156) depends on the material used and can be deposited, for example, to a thickness of about 1 μm . An oxynitride layer can be deposited by, for example, plasma enhanced chemical vapor deposition (PECVD). A BCB layer can be deposited by, for example, spin coating or spray coating.

A second passivation layer (157) is then deposited over the first passivation layer. The second passivation layer (157) reduces the lateral leakage current and is, for example, a high quality oxide or nitride. The thickness of the second passivation layer (157) is not critical, but should be less

than the first passivation layer. The second passivation layer is preferably an oxide with a thickness of about 1000 Å. It is preferably deposited by PECVD.

As shown in FIG. 5b, vias (160) are then opened to expose the source-drain metal (144). Via holes can be opened, for example, by etching through the first and second passivation layers. A metal layer is then deposited so that it contacts the source-drain metal contact. This is followed by deposition of a first doped a-Si layer (148). The first doped a-Si layer (148) can be, for example, N+ doped a-Si. The metal layer and the first doped a-Si layer (148) are then patterned, as shown in FIG. 5c, such that the patterning of the metal layer forms the mushroom shaped collection electrode (146) that defines the pixels.

Then, as shown in FIG. 5d, a continuous layer of i a-Si (150) is deposited. A second doped a-Si layer (152) is deposited over the a-Si layer. The second doped a-Si layer (152) can be, for example, P+ doped a-Si. An upper electrode (154) of, for example, ITO is then deposited over the second doped a-Si layer. The ITO, a-Si, and P+ a-Si are then patterned, preferably in one lithography step.

It will be apparent to those skilled in the art that various modifications and variations can be made in the dual dielectric structure and the method for suppressing lateral leakage current of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

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